REMARKS

This Response is submitted in reply to the Office Action dated December 6, 2004. Claims 1, 2 and 4-15 are pending in the patent application. Claims 1, 2, 4, 5, 6 and 13 have been amended. No new matter has been added by any of the amendments made herein.

Claims 6 and 13 were rejected under 35 U.S.C. § 112. Claim 1, 2 and 4-15 were rejected under 35 U.S.C. § 102(b). Applicants respectfully submit for at least the reasons set forth below, that the rejections has been overcome or are improper. Accordingly, Applicants respectfully request reconsideration of the patentability of Claims 1, 2 and 4-15.

Claims 6 and 13 were rejected under 35 U.S.C. § 112, second paragraph. The Office Action states that Claim 6 includes the element "the information processing apparatus" in line 1 where Claim 1, from which it depends, is a method claim. Similarly, the Office Action states that Claim 13 includes the element "the information processing method" where Claim 10, from which it depends is an apparatus claim. Applicants have amended Claims 6 and 13 to correct these informalities. Accordingly, Applicants respectfully submit that the rejections of Claims 6 and 13 have been overcome.

Claims 1, 2 and 4-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,734,568 to Watanabe et al. ("*Watanabe I*"). Applicants respectfully disagree with and traverse this rejection because *Watanabe* does not disclose, teach, or suggest each and every element of the claimed invention.

Watanabe I is directed to an IC card or smart card which can set security levels for each memory area in the card. (See the Abstract). Specifically as shown in Fig. 4, the memory area includes a plurality of index areas 1 through Y and a plurality of memory areas 1 through Y which correspond to each of the index areas. The index areas are used to access the corresponding memory areas. (Col. 3, lines 20-30). Furthermore, each index area as shown in Fig. 5, includes an area consisting of eight bits for storing different information. Specifically, each index area stores a head address of the corresponding memory area, an area consisting of six bits for setting the security level used to access writing and reading operations of the data stored in the memory area, an area consisting of eight bits for recording a record length in the corresponding memory area, an area for recording the maximum number of records assigned to the memory area and an area for recording the number bytes of the flagged bits located in the

head address. (Col. 3, lines 31-48). The different sections of the index area shown in Fig. 5, each include a predetermined or designated area or number of bits. For example, as described above, the head address is stored in an area consisting of eight bits and the security level is stored in area consisting of six bits. The sizes of these areas in the index area do not vary or are not determined based on the actual amount of information stored in those areas.

Accordingly, *Watanabe I* does not disclose, teach or suggest "a first area for storing data of at least one user and a second area used by said at least one user stored in said first area and managed in a block unit having a predetermined size, and storing plural data for respectively prescribing different access rights to said at least one user in said first area" where the "block unit includes a plurality of blocks that define the size of the memory area associated with each user based on the actual amount of information stored for each user" as defined by amended Claim 1. Claims 2, 3, 4 and 5 each include similar elements to amended Claim 1.

Therefore, for at least the reasons provided above, *Watanabe I* does not disclose, teach or suggest the elements of Claims 1, 2, 4 and 5, and Claims 6-8, 9-13 and 14-15, which depend from these claims, respectively. Accordingly, Claims 1, 2 and 4-15 are each patentably distinguished over *Watanabe I* and are in condition for allowance.

Claims 1, 2 and 4-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,849,614 to Watanabe et al. ("*Watanabe II*"). Applicants respectfully disagree with and traverse this rejection because *Watanabe II* does not disclose, teach, or suggest each and every element of the claimed invention.

Watanabe II is related *Watanabe I* described above and teaches a composite IC card for controlling information of a plurality of different enterprises using the card in which a memory is divided into plurality of storage areas. The IC card also includes a code store section for storing a plurality of codes necessary to access the storage areas. (See the Abstract). Similarly to *Watanabe I, Watanabe II* includes a memory area having a plurality of index areas 1 through X and a plurality of storage areas 1 through X which are associated with each index area. (See Fig. 1). As shown in Fig. 3, each index area is divided into storage area definition information and storage area control information. (Col. 6, lines 42-55). Each storage area includes a first record to Mth record. The information is stored for each record and the record length is predetermined or "before hand set" so as to be written as the storage area definition information

of each index area. Moreover, Fig. 3 indicates that each portion of the index area is a predetermined or predesignated number of bits. For example, the storage area start address is seven bits as shown in Fig. 3.

Accordingly, for the same reasons provided above with respect to *Watanabe I*, *Watanabe II* does not disclose, teach or suggest a first area managed by a block unit where the block unit includes a plurality of blocks that define the size of the memory area associated with each user based on the actual amount of information stored for each user. Therefore, Claims 1, 2 and 4-15 are each patentably distinguished from *Watanabe II* and are in condition for allowance.

In light of the above, Applicants respectfully submit that Claims 1, 2 and 4-15 are patentable over the art of record because neither of the *Watanabe* references discloses, teaches or suggests the elements of these claims. Accordingly, Applicants respectfully request that Claims 1, 2 and 4-15 be deemed allowable at this time and that a timely notice of allowance be issued in this case.

No fees are due in the case. If any other fees are due in connection with this application, the Patent Office is authorized to deduct the fees from Deposit Account No. 02-1818. If such a withdrawal is made, please indicate the attorney docket number (0113235-006) on the account statement.

Respectfully submitted,

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